

(19) World Intellectual Property
Organization
International Bureau



Rec'd PCT/PTO 07 JAN 2005



(43) International Publication Date
22 January 2004 (22.01.2004)

PCT

(10) International Publication Number
WO 2004/008534 A3

(51) International Patent Classification⁷: H01L 27/02

(21) International Application Number:
PCT/IB2003/002873

(22) International Filing Date: 25 June 2003 (25.06.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
02077865.0 12 July 2002 (12.07.2002) EP

(71) Applicant (for all designated States except US): KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants (for US only): VAN DER MEER, Hendrik, H. [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). CUIJPERS, Johannes, L. [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). HUIJSING, Albert, J. [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). AALMERS, Mathijs, A., H. [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). BAYRAM, Eyup [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: DULJVESTIJN, Adrianus, J.; Philips Intellectual Property & Standards, Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,

GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

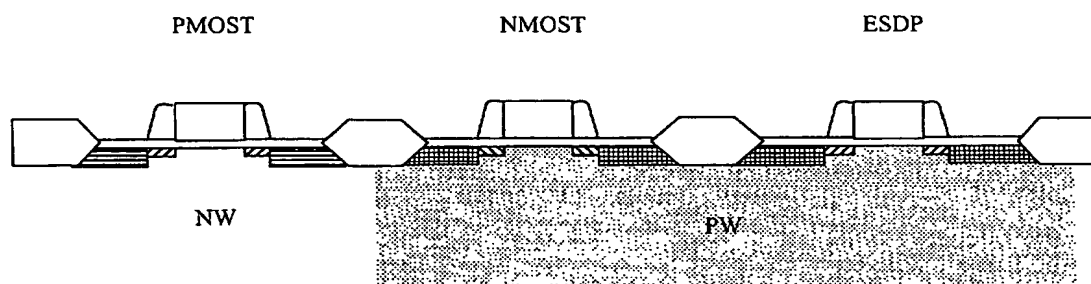
— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

Published:

— with international search report

[Continued on next page]

(54) Title: METHOD OF FORMING AN ELECTROSTATIC DISCHARGE PROTECTING DEVICE AND INTEGRATED CIRCUIT ARRANGMENT COMPRISING SUCH A DEVICE



(57) Abstract: A simple and cost-effective method to improve ESD performance by selectively reducing avalanche breakdown voltage in protection devices by means of locally increasing the acceptor dopant concentration. The present invention relates to an integrated circuit arrangement and method of forming on a semiconductor substrate an electrostatic discharge (ESD) protecting device together with internal circuitry to be protected by said protecting device, wherein an offset transistor arrangement is formed in said protecting device, and an acceptor concentration is increased at said offset transistor arrangement so as to selectively reduce the breakdown voltage of the offset transistor arrangement. The lower breakdown voltage causes the protection devices to trigger at lower voltage during an ESD event, thus protecting the more vulnerable regular LDD transistors.

WO 2004/008534 A3



— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(88) Date of publication of the international search report:
16 December 2004

INTERNATIONAL SEARCH REPORT

Int'l Application No

PCT/IB 03/02873

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L27/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 897 348 A (WU SHYE-LIN) 27 April 1999 (1999-04-27) cited in the application column 2, line 29 - line 63 column 3, line 44 - column 4, line 58 column 5, line 34 - line 45 column 5, line 57 - line 64 figures 1,3,6-8	1-6,10, 11
A	-----	7-9
X	US 6 040 222 A (CHANG YIH-JAU ET AL) 21 March 2000 (2000-03-21) column 2, line 44 - line 63 column 3, line 14 - column 4, line 24 figures 2a-2d ----- -/--	1,2,7-9, 11

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *G* document member of the same patent family

Date of the actual completion of the international search

6 September 2004

Date of mailing of the international search report

12/10/2004

Name and mailing address of the ISA
European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Morena, E

INTERNATIONAL SEARCH REPORT

 Int. Patent Application No.
 P/B 03/02873

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 744 841 A (JAMISON STEPHEN G ET AL) 28 April 1998 (1998-04-28) column 2, line 47 - column 3, line 9 column 4, line 24 - line 30; figures 3-5	1-3,7-9, 11
A	-----	4-6,10
X	US 6 218 226 B1 (LIN GEENG-LIH ET AL) 17 April 2001 (2001-04-17) abstract column 1, line 49 - column 2, line 8 column 2, line 44 - line 53 column 4, line 17 - line 37 figure 2	1,2,7-9, 11
A	-----	1-11
	GROESENEKEN G: "Hot carrier degradation and ESD in submicron CMOS technologies: how do they interact?" ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE SYMPOSIUM PROCEEDINGS 2000 (IEEE CAT. NO.00TH8476) ESD ASSOC ROME, NY, USA, 26 September 2000 (2000-09-26), pages 276-286, XP002295054 ISBN: 1-58537-018-5 the whole document	
A	-----	1-11
	DUVVURY C ET AL: "Reliability design of p<+>-pocket implant LDD transistors" INTERNATIONAL ELECTRON DEVICES MEETING 1990. TECHNICAL DIGEST (CAT. NO.90CH2865-4) IEEE NEW YORK, NY, USA, 9 December 1990 (1990-12-09), pages 215-218, XP002295055 the whole document	

INTERNATIONAL SEARCH REPORT

Int. Application No

IB 03/02873

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5897348	A	27-04-1999	NONE		
US 6040222	A	21-03-2000	NONE		
US 5744841	A	28-04-1998	US JP	5733794 A 8241996 A	31-03-1998 17-09-1996
US 6218226	B1	17-04-2001	US	2001010954 A1	02-08-2001